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EXAMINER
PARIHAR, SUCHIN

ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

Office Action Summary	Application No.	Applicant(s)
	10/622,923	BAECKLER ET AL.
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/30/2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   This FINAL office action is in response to application 10/622,923, amendment

filed 11/30/2006. Claims 14-22 are currently amended. Claims 1-22 are pending in this

application.

2.   Applicant's arguments filed 11/30/2006 have been fully considered but they are

not persuasive. The applicable rejections from the prior office action are incorporated

herein.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4.   **Claims 1, 9, 10, 12, 14 and 21 are rejected under 35 U.S.C. 102(e)** as being

anticipated by Wallace (US PG Pub 2006/0117280).

5.   With respect to claims 1 and 14, Wallace teaches a method and computer

system (see Figure 11) that combines look-up tables (see paragraph [0135]) in a design

for programmable integrated circuit (see paragraph [0135]) comprising: selecting first

and second LUTs from the design (i.e. identifying the inputs of first and second XOR

gates, paragraph [0025]); determining whether both of the LUTs implement a same

function (i.e. implement the same logic function, paragraph [0006]); and if the first and

second LUTs implement the same function, combining masks of the LUTs into a shared

LUT mask in the design (i.e. if two functions are the same, then merge them, paragraph

[0092]).

6.   With respect to claim 9, Wallace teaches all the elements of claim 1, from which

the claim depends. Wallace teaches: wherein determining if the LUTs both perform the

same function further comprises: determining if an output value of the first LUT equals

an output value of the second LUT for each possible input value that is applied to the

input terminals of both of the LUTs (i.e. two gates [LUTs] are said to be equivalent if the

outputs do not change if any of the inputs are interchanged, paragraph [0024]).

7.   With respect to claim 10, Wallace teaches all the elements of claim 1, from which

the claim depends. Wallace teaches: selecting third and fourth LUTs from the design

(i.e. identifying the inputs of first and second XOR gates, paragraph [0025]); determining

whether both of the LUTs implement a same function (i.e. implement the same logic

function, paragraph [0006]); and if the third and fourth LUTs implement the same

function, combining masks of the LUTs into a shared LUT mask in the design (i.e. if two

functions are the same, then merge them, paragraph [0092]).

8.   With respect to claims 12 and 21, Wallace teaches all the elements of claims 1

and 14, from which the claims depend respectively. Wallace teaches: breaking apart

the mask of the LUTs (i.e. disjoint-support decomposition into simpler functions,

paragraph [0047]) if the mask lies in a critical path in the design (minimize logic levels

from the critical path, paragraph [0039]) and placing the first and second LUTs into

different logic elements (i.e. multi-gate, paragraph [0039]) within the design.

Claim Rejections - 35 USC § 103

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

10.   **Claims 2-6, 11 and 15-19 are rejected under 35 U.S.C. 103(a)** as being

unpatentable over Wallace (US PG Pub 2006/0117280) in view of Andreev et al.

(6,848,094). With respect to claims 2-6, 11, and 15-19, Wallace teaches all the

elements of claims 1 and 14, from which the claims depend respectively. Wallace fails

to specifically teach a method/system wherein input signals are rearranged iteratively in

order to determine whether two LUTs implement the same function. However, Andreev

teaches a method of determining whether two LUTs implement the same function (Col

1, lines 5-12) wherein the order of input signals the LUTs are rearranged in order to

determine whether both LUTs implement the same function (Col 1, lines 20-34). It

would have been obvious to one of ordinary skill in the art to incorporate Andreev into

the method of Wallace because Andreev suggests that the re-ordering of inputs and

corresponding outputs is helpful in removing redundant circuits, i.e. determining whether

two LUTs implement the same function (Col 1, lines 20-35).

11.   With respect to claim 2, Wallace teaches all the elements of claim 1, from which

the claim depends, wherein. Andreev teaches a method of determining whether two

LUTs implement the same function (Col 1, lines 5-12) wherein common input signals of

LUTs are identified, and the order of input signals of one of the LUTs are rearranged so

that the common input signals are applied to a corresponding input terminal in both of

the LUTs, and this method determines whether both LUTs implement the same function

based on the first rearranged order of input signals (Col 1, lines 20-34).

12. With respect to claim 3, Wallace in view of Andreev teaches all the elements of

claim 2, from which the claim depends, wherein. Andreev teaches a method of

determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein

the order of at least two uncommon input signals of one of the LUTs are rearranged with

respect to the input terminals of that LUT, and this method determines whether both

LUTs implement the same function (Col 1, lines 20-34).

13. With respect to claim 4, Wallace teaches all the elements of claim 1, from which

the claim depends, wherein. Andreev teaches a method of determining whether two

LUTs implement the same function (Col 1, lines 5-12) wherein the order of at least two

input signals of one of the LUTs are rearranged with respect to the input terminals of

that LUT, and this method determines whether both LUTs implement the same function

(Col 1, lines 20-34).

14. With respect to claim 5, Wallace in view of Andreev teaches all the elements of

claim 4, from which the claim depends. Wallace teaches: if the LUTs implement the

same function with the first rearranged order (i.e. input pin swap [rearrangement]

equivalence, paragraph [0036]), combining the masks of the LUTs into a shared LUT

mask in the design (i.e. merge the two functions into one function, paragraph [0092]).

Andreev teaches a method of determining whether two LUTs implement the same

function (Col 1, lines 5-12) wherein the order of at least two input signals of one of the

LUT's are rearranged with respect to the input terminals of that LUT, and this method determines whether both LUTs implement the same function (Col 1, lines 20-34).

15.   With respect to claim 6, Wallace in view of Andreev teaches all the elements of claim 5, from which the claim depends. Andreev teaches a method for determining whether two LUTs implement the same function (Col 1, lines 5-12). Betz teaches a method wherein two LUTs are combined into a shared mask (Col 1, lines 11-13, i.e. combining functional blocks into fewer programmable circuit elements) if it is determined that the LUTs are combinable (i.e. implement same function, as suggested by Andreev: Col 1, lines 7-10). Andreev also teaches rearranging the order of at least two input signals of the first LUT with respect to the input terminals of that LUT because it has not yet been determined that the LUT's implement the same function.

16.   With respect to claim 11, Wallace teaches all the elements of claim 10, from which the claim depends, wherein. Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein the order of at least two input signals of one of the LUTs are rearranged with respect to the input terminals of that LUT if previous rearrangements of input signals to not determine same function (Col 1, lines 20-34).

17.   With respect to claim 15, Wallace teaches all the elements of claim 14, from which the claim depends. Andreev teaches a computer system wherein at least some integer N of common input signals for the first and second LUT are determined, and the order of input signals of one of the LUTs are rearranged so that the common input signals are applied to a corresponding input terminal in both of the LUTs, in the same

order, to provide a first rearranged order, and this method determines whether both

LUTs implement the same function (Col 1, lines 20-34).

18.   With respect to claim 16, Wallace in view of Andreev teaches all the elements of

claim 15, from which the claim depends, wherein. Andreev teaches a computer system

wherein the code is provided for rearranging an order of at least two uncommon input

signals with respect to input terminals of one of the LUTs to provide a second

rearranged order, if the LUTs do not implement the same function (Col 1, lines 20-34).

Kelsey teaches a computer system (Col 3, lines 10-12, i.e. Computer Aided Engineering

Tool) which includes code to compare output values of the LUTs to determine if the

LUTs generate the identical function based on the second rearranged order of the input

signals (Col 2, lines 28-33).

19.   With respect to claim 17, Wallace teaches all the elements of claim 14, from

which the claim depends, wherein. Andreev teaches a computer system (Col 7, lines

57-60, i.e. computer program of the present invention) wherein code is provided to

determine whether two LUTs implement the same function (Col 1, lines 5-12) which

involves the rearrangement of the order of at least two input signals of one of the LUTs

with respect to the input terminals of that LUT (Col 1, lines 20-34).

20.   With respect to claim 18, Wallace in view of Andreev teaches all the elements of

claim 17, from which the claim depends, wherein. Andreev teaches a computer system

(Col 7, lines 57-60, i.e. computer program of the present invention) wherein code is

provided for combining masks of the LUTs (Col 1, lines 10-12, i.e. removing redundant

circuits) in the design if the LUTs implement the identical function with the first

rearranged order (Col 1, lines 23-25, i.e. re-ordering inputs), and code for rearranging

the order of input signals of the LUTs with respect to the input terminals of that LUT to

provide a second rearranged order of the input signals, if the LUTs do not implement

the identical function with the first rearranged order (Col 1, lines 20-34)).

21.   With respect to claim 19, Wallace in view of Andreev teaches all the elements of

claim 18, from which the claim depends, wherein. Andreev teaches a computer system

(Col 7, lines 57-60, i.e. computer program of the present invention) wherein code is

provided for combining masks of the LUTs (Col 1, lines 10-12, i.e. removing redundant

circuits) in the design if the LUTs implement the identical function with the second

rearranged order (Col 1, lines 23-25, i.e. re-ordering inputs), and code for rearranging

the order of input signals of the LUTs with respect to the input terminals of that LUT to

provide a third rearranged order of the input signals, if the LUTs do not implement the

identical function with the second rearranged order (Col 1, lines 20-34)).

22.   **Claim 22 is rejected under 35 U.S.C. 103(a)** as being unpatentable over

Wallace (US PG Pub 2006/0117280) in view of Andreev et al. (6,848,094) and in further

view of Harrison et al. (5,636,368).

23.   With respect to claim 22, Wallace in view of Andreev teaches all the elements of

claim 18, from which the claim depends. Wallace in view of Andreev does not teach:

code for determining if the LUTs have at least N common input signals, after the output

values of the LUTs have been compared; code for determining if the LUTs have no

more than M unique input signals, after the output values of the LUTs have been

compared, wherein the masks of the first and second LUTs are not combined if the

LUTs have less than N common input signals or more than M unique input signals,

wherein N and M are integers. However, Harrison teaches: code for determining if the

LUTs have at least N common input signals (i.e. at Fig 8 step 820, it is determined

whether the LUT-implemented function block [see Col 16, lines 23-25 for "look-up

table"] contains at least 21 inputs), after the output values of the LUTs have been

compared; code for determining if the LUTs have no more than M unique input signals

(i.e. at Fig 8 step 830, it is determined whether the LUT-implemented function block

[see Col 16, lines 23-25 for "look-up table"] contains more than 21 inputs), after the

output values of the LUTs have been compared, wherein the masks of the first and

second LUTs are not combined if the LUTs have less than N common input signals or

more than M unique input signals (i.e. dividing LUT-implemented function block

equation into two or more sub-expressions, see Fig 8, step 840), wherein N and M are

integers.

It would have been obvious to one of ordinary skill in the art to incorporate

Harrison into the invention of Wallace and Andreev for at least the following reasons:

Harrison improves the invention of Wallace by providing an alternative way to determine

whether representations of digital circuits (i.e. logic equations, see Harrison, Col 11,

lines 42-45) can be converted into layouts for circuit implementation (i.e. determining

whether a logic equation is implementable in a function block [FFB], see Harrison, Col

11, lines 42-45). Note that in paragraph [0003] of Wallace, Wallace recites: "this

invention relates to techniques for converting representations of digital circuits, such as

logic diagrams [i.e. diagrams which can be expressed by logic equations] or

schematics, into layouts for circuit implementation."

24.   **Claims 7, 8, 13 and 20 are rejected under 35 U.S.C. 103(a)** as being

unpatentable over Wallace (US PG Pub 2006/0117280) in view of Harrison et al.

(5,636,368).

25.   With respect to claim 7, Wallace teaches all the elements of claim 1, from which

the claim depends. Wallace does not teach: before determining whether the LUTs

implement the same function, determining if the LUTs have at least N common input

signals; and if the LUTs do not have at least N common input signals, preventing the

masks of the LUTs from being combined, wherein N is an integer. However, Harrison

teaches: before determining whether the LUTs implement the same function,

determining if the LUTs have at least N common input signals (i.e. at Fig 8 step 820, it is

determined whether the LUT-implemented function block [see Col 16, lines 23-25 for

"look-up table"] contains at least 21 inputs); and if the LUTs do not have at least N

common input signals (direction of 'N' below step 820 of Fig 8, i.e. LUT-implemented

function block does not have at least 21 inputs), preventing the masks of the LUTs from

being combined (i.e. dividing LUT-implemented function block equation into two or more

sub-expressions, see Fig 8, step 840), wherein N is an integer. It would have been

obvious to one of ordinary skill in the art at the time of the invention to incorporate

Harrison into the invention of Wallace for at least the following reasons: Harrison

improves the invention of Wallace by providing an alternative way to determine whether

representations of digital circuits (i.e. logic equations, see Harrison, Col 11, lines 42-45)

can be converted into layouts for circuit implementation (i.e. determining whether a logic

equation is implementable in a function block [FFB], see Harrison, Col 11, lines 42-45).

Note that in paragraph [0003] of Wallace, Wallace recites: "this invention relates to

techniques for converting representations of digital circuits, such as logic diagrams [i.e.

diagrams which can be expressed by logic equations] or schematics, into layouts for

circuit implementation."

26.   With respect to claim 8, Wallace in view of Harrison teaches all the elements of

claim 7, from which the claim depends. Wallace does not teach: before determining

whether the LUTs implement the same function, determining if the LUTs have more

than M unique input signals; and if the LUTs have more than M unique input signals,

preventing the masks of the LUTs from being combined, wherein M is an integer.

However, Harrison teaches: before determining whether the LUTs implement the same

function, determining if the LUTs have more than M unique input signals (i.e. at Fig 8

step 830, it is determined whether the LUT-implemented function block [see Col 16,

lines 23-25 for "look-up table"] contains more than 21 inputs); and if the LUTs have

more than M unique input signals (direction of 'N' below step 830 of Fig 8, i.e. LUT-

implemented function block has more than 21 inputs), preventing the masks of the LUTs

from being combined (i.e. dividing LUT-implemented function block equation into two or

more sub-expressions, see Fig 8, step 840), wherein M is an integer.

27.   With respect to claim 13, Wallace teaches all the elements of claim 1, from which

the claim depends. Wallace does not teach: after determining whether both of the LUTs

implement the same function, determining if the LUTs have at least N common input

signals; and determining whether the LUTs have no more than M unique input signals,

wherein the LUT masks are combined into the shared LUT mask only if the LUTs have

at least N common input signals and no more than M unique input signals, wherein N

and M are integers. However, Harrison teaches: after determining whether both of the

LUTs implement the same function, determining if the LUTs have at least N common

input signals (i.e. at Fig 8 step 820, it is determined whether the LUT-implemented

function block [see Col 16, lines 23-25 for "look-up table"] contains at least 21 inputs);

and determining whether the LUTs have no more than M unique input signals (i.e. at Fig

8 step 830, it is determined whether the LUT-implemented function block [see Col 16,

lines 23-25 for "look-up table"] contains more than 21 inputs), wherein the LUT masks

are combined into the shared LUT mask only if the LUTs have at least N common input

signals and no more than M unique input signals (step 840 of Fig 8 is bypassed, i.e.

equation is not split into two sub-expressions, i.e. one shared LUT-implemented

function block), wherein N and M are integers. It would have been obvious to one of

ordinary skill in the art at the time of the invention to incorporate Harrison into the

invention of Wallace for at least the following reasons: Harrison improves the invention

of Wallace by providing an alternative way to determine whether representations of

digital circuits (i.e. logic equations, see Harrison, Col 11, lines 42-45) can be converted

into layouts for circuit implementation (i.e. determining whether a logic equation is

implementable in a function block [FFB], see Harrison, Col 11, lines 42-45). Note that in

paragraph [0003] of Wallace, Wallace recites: "this invention relates to techniques for

converting representations of digital circuits, such as logic diagrams [i.e. diagrams

which can be expressed by logic equations] or schematics, into layouts for circuit

implementation."

28.   With respect to claim 20, Wallace teaches all the elements of claim 14, from

which the claim depends. Wallace does not teach: code for determining if the LUTs

have at least N common input signals; and code for determining if the LUTs have no

more than M unique input signals, wherein implementation of the code for comparing

the output values of the first and second LUTs is prevented if the first and second LUTs

have less than N common input signals or more than M unique input signals, wherein N

and M are integers. However, Harrison teaches: code for determining if the LUTs have

at least N common input signals (i.e. at Fig 8 step 820, it is determined whether the

LUT-implemented function block [see Col 16, lines 23-25 for "look-up table"] contains at

least 21 inputs); and code for determining if the LUTs have no more than M unique input

signals (i.e. at Fig 8 step 830, it is determined whether the LUT-implemented function

block [see Col 16, lines 23-25 for "look-up table"] contains more than 21 inputs),

wherein implementation of the code for comparing the output values of the first and

second LUTs is prevented if the first and second LUTs have less than N common input

signals or more than M unique input signals, wherein N and M are integers (i.e. dividing

LUT-implemented function block equation into two or more sub-expressions, see Fig 8,

step 840). It would have been obvious to one of ordinary skill in the art at the time of

the invention to incorporate Harrison into the invention of Wallace for at least the

following reasons: Harrison improves the invention of Wallace by providing an

alternative way to determine whether representations of digital circuits (i.e. logic

equations, see Harrison, Col 11, lines 42-45) can be converted into layouts for circuit

implementation (i.e. determining whether a logic equation is implementable in a function

block [FFB], see Harrison, Col 11, lines 42-45). Note that in paragraph [0003] of

Wallace, Wallace recites: "this invention relates to techniques for converting

representations of digital circuits, such as logic diagrams [i.e. diagrams which can be

expressed by logic equations] or schematics, into layouts for circuit implementation."

Response to Arguments

29.   Applicant's arguments filed 11/30/2006 have been fully considered but they are

not persuasive. Examiner's response to arguments follows below.

30.   Applicant asserts that Wallace fails to teach or suggest: determining whether

both of the LUTs implement a same function. Examiner disagrees with this assertion.

31.   Examiner points out that Wallace teaches: determining whether both of the LUTs

implement a same function (i.e. logic gates that implement the same logic function,

paragraph [0006]). Wallace's discussion of logic gates that implement the same logic

function is enough to suggest the determination of whether both LUTs implement a

same function. Examiner points out that Applicant's specification describes a LUT as a

small binary circuit [i.e. logic gate(s)] in paragraph [0003] of Applicant's specification.

32.   Applicant asserts that Wallace fails to teach or suggest: combining masks of the

LUTs into a shared LUT mask in the design. Examiner disagrees with this assertion.

33.   Examiner points out that Wallace teaches: combining masks of the LUTs into a

shared LUT mask in the design (two functions that are merged into a larger function,

paragraph [0092]). Examiner also points out that Wallace's discussion of merging [i.e.

combining] two functions that implement the same functionality in conjunction with Wallace's discussion of placing schematics into layouts for circuit implementation [i.e. mask design] is enough to suggest: combining masks of the LUTs into a shared LUT mask in the design.

34.   Applicant asserts that Andreev fails to teach or suggest: rearranging input signals to the input terminals of a LUT and determining if both LUTs implement the same function based on the rearrangement. Examiner disagrees with this assertion.

35.   Examiner points out that Andreev teaches: rearranging input signals to the input terminals of a LUT (re-ordering the inputs of the logic elements, see Andreev, Col 1, lines 20-35) and determining if both LUTs implement the same function based on the rearrangement (determining output equivalency, see Andreev, Col 1, lines 20-35).

36.   Applicant asserts that Harrison fails to teach or suggest: determining the number of common or non-common inputs of two LUTs or preventing the masks from being combined. Examiner disagrees with this assertion.

37.   Examiner points out that Harrison teaches: determining the number of common or non-common inputs of two LUT (i.e. at Fig 8 step 820, it is determined whether the LUT-implemented function block [see Col 16, lines 23-25 for "look-up table"] contains at least 21 inputs) or preventing the masks from being combined (i.e. dividing LUT-implemented function block equation into two or more sub-expressions, see Fig 8, step 840).
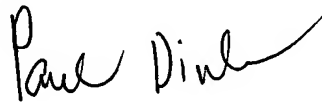
Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER